MITEL
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AN4883

NWK939 Layout Application Information

Preliminary Information

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OVERVIEW

This document provides a description of PCB layout considerations for the NWK939 10BASE-T/ 100BASE-TX Physical Layer Device. The objective of the document is to help you successfully implement the NWK939 in your High Speed Network Design. While these recommendations result from successful designs in our labs, there are numerous ways to implement high speed designs. Because of the sensitivity of high speed circuitry, ALL connections to NWK939 should be routed with care.

NWK939 INTERFACE CONNECTIONS

NWK939 to PCS Layer

The NWK939 has two distinct interfaces. One interface provides connections to a device providing the PCS Layer functions as outlined in the 802.3u specification. Common devices incorporating the PCS function are the DEC21143 LAN Controller and the NWK960 LAN Controller. Careful attention is necessary when routing the clock signals in order to help reduce skew, noise and the potential for cross-talk. It is recommended to keep clock lines as short as possible with a minimum .050 inch spacing from other signals. The clock signals should be routed first in order to help maintain the necessary spacing. It is also recommended to avoid routing clock lines directly underneath the device. The TDAT<4:0> and RDAT<4:0> lines need to be kept short as possible, similar in length, and have common characteristics. This is necessary as each line is sampled by their respective clocks (TXC & RXC) and when combined, make up a “5 Bit Symbol” as defined in the TP-PMD specification.

NWK939 to Network

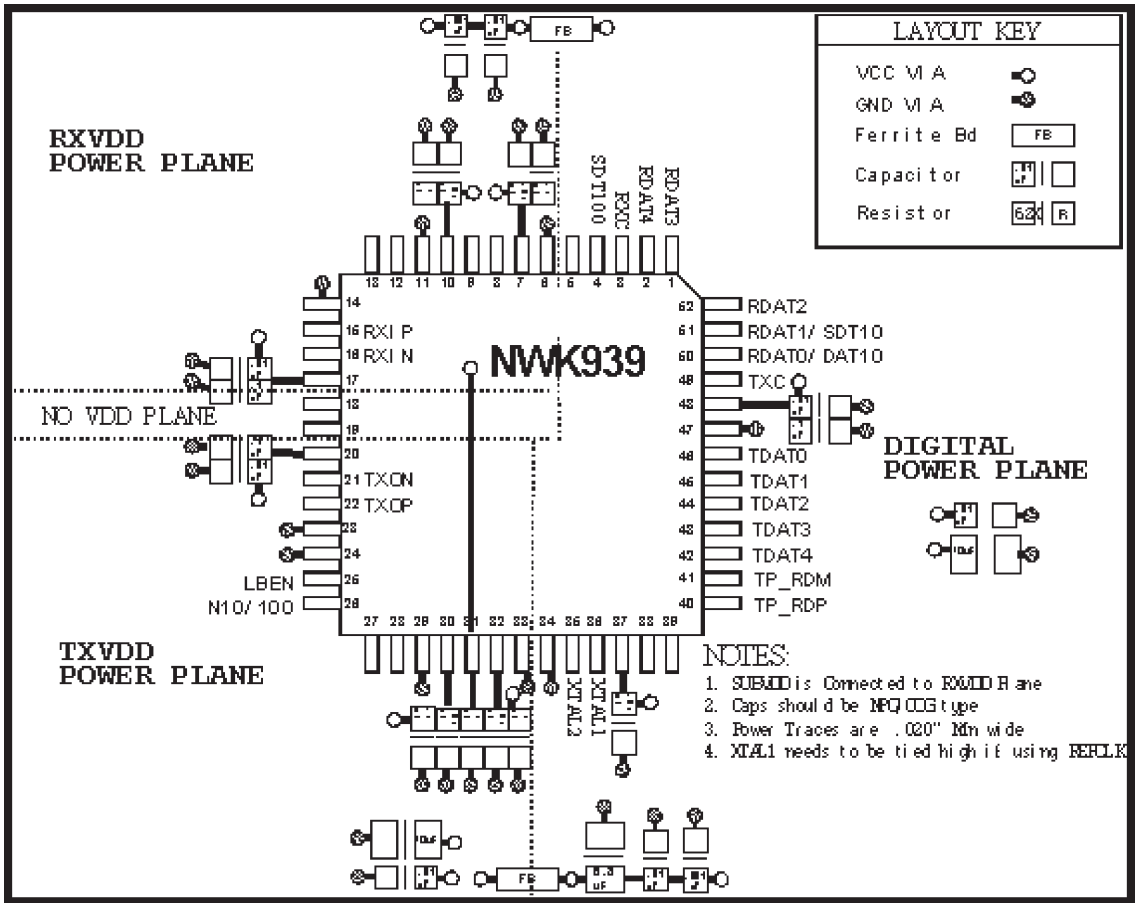
The second interface connects the NWK939 to the RJ45 connector via the magnetic. This area is especially sensitive. Two pairs of differential Analog signals (RXIP/N & TXOP/N) make up this interface. Both pairs of signals should be kept as short and straight as possible. The RX lines are especially sensitive to extraneous noise, and should be routed using the shortest path. If a trade-off is necessary between RX and TX when placing components, the RX path should receive the cleanest path. The TX and RX lines must be routed as pairs with as little difference between the two lines in each pair. You should have even spacing between each of the 2 signals at all times. Do not route the TX and RX signals pairs near each other. Try to maintain a .050 inch minimum spacing from any TX or RX line. You should also avoid routing other signals such as LED indicator signals near the RX or TX pairs (maintain a .050 inch minimum spacing from any TX line or RX line). Both the TX and RX pairs should never cross a voided plane on an adjacent pcb layer. The RX traces should have a differential characteristic impedance of 100 Ohms to provide effective coupling to the UTP Cable, then be properly terminated to eliminate reflections from the incoming signal. The RX termination resistors should be located as close to the pins as possible. The differential characteristic impedance of the TX pair is determined by the type of magnetic you choose for your design. We suggest a magnetic with a 1:1 Ratio on both the TX and RX pairs. This provides effective coupling to the Network by matching the impedance of the traces to the impedance of the cable.

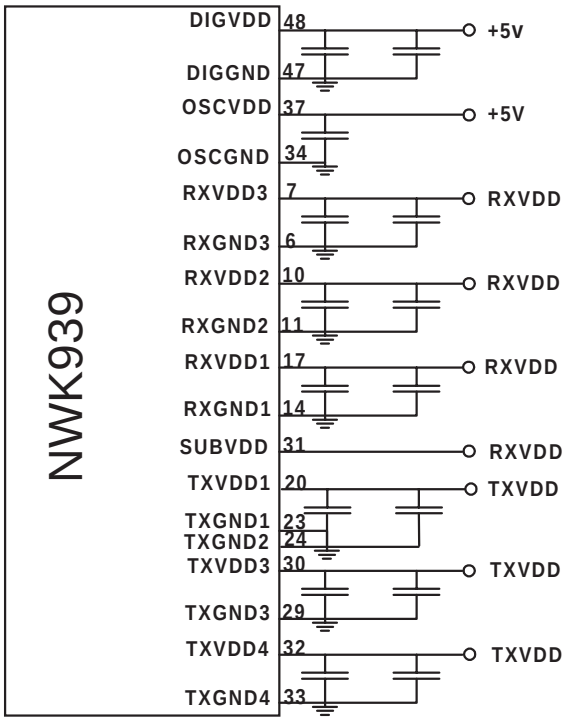
Power Supply Decoupling

Decoupling of power supplies is very important to help ensure the success of the design. Values for the decoupling components are shown in the schematic diagram. The values, locations, and number of components shown represent known working conditions for the NWK939. Based on your application alternative decoupling schemes may be necessary, including less decoupling or different values than those shown in the diagram. Please refer to layout diagram for details on the decoupling components locations.

Power Supply Grouping

When connecting the various power supplies to the NWK939 it is important to reduce noise coupling. The intent of the layout diagram is to demonstrate locating the decoupling devices close to the VDD power pins. While we recommend a Solid Ground plane on an internal board layer, there are many methods which have been successfully implemented. Using a solid ground plane enables the circuit to have short, low impedance paths to ground. Connections from the power pins to the planes should use wide traces. To further reduce cross-talk we recommend splitting the VDD Power Planes into three sections. The digital or TTL plane (DIGVDD), a Transmit VDD plane (TXVDD), and a Receive VDD plane (RXVDD). You need to ensure the decoupling devices are connected to the respective power plane.





NWK939 Power Supply Decoupling

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